

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTORNEY DOCKET NO.
1454.1210

APPLICATION NO.

FIRST NAMED INVENTOR

Peer JOHANNSEN

FILING DATE

1/8/02

GROUP ART UNIT
285JC971 U.S. PATENT OFFICE
10/03 870
01/08/02

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						

OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

PD	AB	Cyrluk, et al.; "An Efficient Decision Procedure for the Theory of Fixed-Sized Bit-Vectors", CAV '97, pp. 6-71, 1997
	AC	Barrett et al., "Validity Checking for Combinations of Theories with Equality"; FMCAD '96, pp. 187-201, 1996
	AD	Barrett et al., "A Decision Procedure for Bit-Vector Arithmetic", DAC '98 pp. 522-527, 1998
	AE	Bryant et al., "Exploiting Positive Equality in a Logic of Equality with Uninterpreted Functions, CAV '99 pp. 470-482, 1999
	AF	Bjørner et al, "Deciding Fixed and Non-fixed Size Bit-vectors", TACAS '98, pp. 376-392, 1998
	AG	Velev et al., "Exploiting Positive Equality and Partial Non-Consistency in the Formal Verification of Pipelined Microprocessors", DAC '99, pp. 397-401, 1999
	AH	Velev et al., "Bit-Level Abstraction in the Verification of Pipelined Microprocessor by Correspondence Checking", FMCAD '98, pp. 18-35 1998
	AI	Huang et al., "Assertion Checking by Combined Word-Level ATPG and Modular Arithmetic Constraint-Solving Techniques", DAC '00, pp. 118-123, 2000
	AJ	Cyrluk, et al.; "An Efficient Decision Procedure for the Theory of Fixed-Sized Bitvectors with Composition and Extraction", Technical Report No. UIB-96-8 (Ulmer Informatik-Berichte 96-08), Fakultät für Informatik, Universität Ulm, 1996
	AK	Levitt, "Formal Verification Techniques for Digital Systems", PhD Thesis at the Department of Electrical Engineering, Stanford University, 1998
	AL	Silva, "Search Algorithms for Satisfiability Problems in Combinational Switching Circuits", PhD Thesis, University of Michigan, 1995
	AM	Silva et al., "Boolean Satisfiability Algorithms and Applications in Electronic Design Automation", CAV '00, Invited Tutorial, 2000
	AN	Möller, "A Decision Procedure for Hardware Verification", Diploma Thesis, University of Ulm, 1998
PD	AO	Möller et al., "Solving Bit-Vector Equations", FMCAD '98, pp. 36-48, 1998

EXAMINER

PAUL DINH

DATE CONSIDERED

3/28/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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